REMARKS

Applicant herewith submits a Second Amendment After Final Action in response to the Examiner's Advisory Action of June 16, 2004.

Applicant acknowledges with gratitude that the rejections of claims 4 and 17-21 under 35 U.S.C. § 112 have been withdrawn. Applicant respectfully disagrees wth the Advisory Action regarding the rejections of the remaining claims, however, for the following reasons, and requests reconsideration.

According to the advisory action, the drawings remain objected to for claim 2 because they fail to disclose a control means under control of a shift clock for the first n-bit shift register. Applicant respectfully disagrees. Fig. 2, which shows control circuit 101, is a second n-bit shift register containing S_1 – Sn. Also as shown in Fig. 2, control circuit 101 is fed by the clock "clk." Referring now to Fig. 1, "clk" – which is the same clock sent to control circuit 101 – fed to the first n-bit shift register, D_1-Dn. To reinforce this, the specification provides that "clock signal (CLK) 106 is inputted to each of the bit registers of . . . shift register 102 . . . . The clock signal 106 is also inputted to the control circuit 101, which is operated under control of system clock." (Pages 10-11.) As a result, the drawings do disclose a control means [101] under control of a shift clock ["clk"] for the first n-bit shift register [102]. For the above reasons, the objection should be withdrawn.

Claim 2 remains rejected based on Hidemitsu, J.P. 411088119A. According to the Advisory Action:

> Figure 11 is an control mean to generate a selection signals (S1-S5) that would be used in Figure 7 for selecting data accordingly. In general, Hidemitsu clearly discloses the limitation "a second n-bit shift register (108-113) for shifting a ramp-up/down signal (e.g. T2) through successive bits stages under control of a shift clock for the first n-bit shift register' in figures 11 and 7.

Applicant respectfully disagrees. Assuming for the sake of argument that the Advisory Action is correct, "n" = 6. That is, the second n-bit shift register of Fig. 11 has six bits, i.e., items 108-113. However, Fig. 11 discloses only five control signals, S1-S5, whereas Applicant claims "n" control signals. For the Advisory Action to be correct, there must be six control signals (because n=6), but Hidemitsu shows only five control signals. Also, the first n-bit shift register in Fig. 7 shows only four bits (items 2-5), whereas Applicant claims an "n-bit" shift register. Again, for the Advisory Action to be correct, the shift register must hold six bits (because n=6), but Hidemitsu shows only four bits.

For the reasons above, claim 2 is patentable over Hidemitsu. Withdrawal of the rejection of claim 2 over Hidemitsu is thus respectfully requested.

The Advisory Action states that claim 10 is rejected under the same rationale as claim 2. For the reasons above, claim 10 is patentable over Hidemitsu.

Finally, the Advisory Action maintains the rejection for claim 17 because:

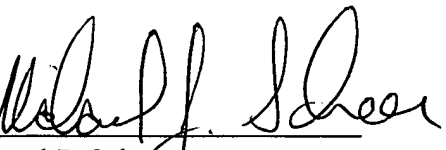
> Applicant argued that the cited reference fails to teach or suggest EITHER the fixed value or the FIR filter coefficient. In Figure 1, the control mean (22) outputs selection signals that are used to select either input shift data or a fixed value "0" (e.g. 6-10).

Applicant respectfully disagrees. A FIR filter coefficient cannot be selected based on Hidemitsu's control means (22), which outputs either input data or a fixed value "0", because it is not an input. Claim 17 requires "each switch selecting either the fixed value or the FIR filter coefficient depending upon the control circuit output signal". As the Advisory Action acknowledges, Hidemitsu's switch can select either the input data or "0", not a FIR filter coefficient as claimed.

In view of the above, reconsideration is requested as each of the presently pending claims in this application is believed to be in immediate condition for allowance and such action is earnestly solicited.

Dated: July 14, 2004

Respectfully submitted,

By 

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